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**BONDING AN INTERCONNECT TO A CIRCUIT DEVICE AND  
RELATED DEVICES**

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## **Bonding an Interconnect to a Circuit Device and Related Devices**

### **TECHNICAL FIELD**

**[0001]** This invention relates to bonding of interconnects to circuit devices.

### **BACKGROUND**

**[0002]** A circuit device typically communicates electrically through “interconnects.” Interconnects are so named because they allow circuit devices to electrically connect with other circuit elements. Interconnects often include an arrangement of conductive wires to electrically connect a circuit device. Use of circuit devices that are small or densely packed (“dense circuit devices”), however, can be limited because of difficulties in bonding interconnects to such devices.

**[0003]** By way of example and referring to Figure 1, a side-section view of a fragment of a dense circuit device is indicated generally by reference numeral 102. The device 102 includes electrical bond pads 104. The pads 104 have a width 106 and are generally separated from each other by a space 108. The smaller or denser the device 102, typically the less the width 106 and the space 108. As the width 106 and space 108 of the pads 104 get smaller and smaller with production of smaller or denser circuit devices, forming interconnections among and between these devices becomes more and more difficult.

**[0004]** Again referring to Figure 1, a side-section view of a fragment of a conventional interconnect is indicated generally by reference numeral 110. The conventional interconnect 110 is typically made of different materials than the device 102, often because the materials used in the device 102 are relatively expensive. Also typically, to bond the conventional interconnect 110 to the pads 104 of the device 102, heat is used.

**[0005]** But a significant problem can occur when using heat to bond the conventional interconnect 110 to the pads 104 of the device 102. If the coefficient of thermal expansion (called “CTE”) for the conventional interconnect

110 and the device 102 are even slightly different, wires 112 of the conventional interconnect 110 may not match up with the pads 104 when they are heated for bonding. When the width 106 or the space 108 is very small, the wires 112 may completely miss the pads 104 or line up with the wrong ones.

**[0006]** By way of example and referring to Figure 2, a side sectional view of the device 102 and the conventional interconnect 110 when each is heated is shown. Both the device 102 and the conventional interconnect 110 are shown expanded in this example, but the expansion of the conventional interconnect 110 does not match the expansion of the device 102. As shown, the wires 112 do not properly match up with the pads 104. When the width 106 or the space 108 is very small, such as less than 100 nanometers, and the device 102 or the interconnect 110 is significantly larger than the width 106 or the space 108, a difference in coefficient of thermal expansion between the device 102 and the conventional interconnect 110 may cause the pads 104 and the wires 112 to not match up with each other. If, for instance, a coefficient of thermal expansion between the device 102 and the interconnect 110 is different by five percent, the wires 112 and the pads 104 may miss each other by hundreds and hundreds of nanometers. This failure of conventional heat bonding may make it impractical or unusable for interconnecting to some dense circuit devices.

**[0007]** Other prior-art techniques for bonding an interconnect to a circuit device can also cause various problems. Eutectic bonding, for instance, can require use of specific, non-optimal materials for the wires 112 and/or the bond pads 104. These non-optimal materials can limit the usability of the dense circuit device 102, because they may not be highly conductive, which is especially important with small-scale interconnects used with dense circuit devices. This eutectic bonding technique can also fail by providing too weak an electrical connection between the bond pads 104 and the wires 112.

**[0008]** Further, these and other typical techniques for electrically bonding the conventional interconnect 110 to the circuit device 102 include mechanical bonding of the wires 112 to the bond pads 104. This can cause a significant problem. If the device 102 and the conventional interconnect 110 are subject to heat, CTE mismatch of the wires 112 to the bond pads 104 can cause the

mechanical bonding between them to fail. This mechanical failure often causes the electrical connection between the wires 112 and the bond pads 104 to also fail.

**[0009]** There is, therefore, a need for a technique for bonding interconnects to dense circuit devices that reduces CTE-related problems, and is reliable, less expensive, and/or more production-friendly than permitted by present-day techniques.

### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side-section view along a depth and width dimension of a prior-art dense circuit device and prior-art interconnect, and is discussed in the "Background" section above.

Fig. 2 is a view of the dense circuit device and the interconnect of Fig. 1 after each is heated.

Fig. 3 is a side-section view along a depth and length dimension of one embodiment of a dense circuit device with electrical bond pads.

Fig. 4 is a view of the Fig. 3 dense circuit device and a spacer substrate.

Fig. 5 is a view of the Figs. 3 and 4 dense circuit device and the Fig. 4 spacer substrate bonded together.

Fig. 6 is a view of the Fig. 5 dense circuit device and spacer substrate and an embodiment of an electrical interconnect.

Fig. 7 is a bottom plan view along a length and width dimension of the Fig. 6 dense circuit device and spacer substrate.

Fig. 8 is a top plan view along a length and width dimension of the Fig. 6 electrical interconnect.

Fig. 9 is a view of the Fig. 6 dense circuit device, spacer substrate, and electrical interconnect and an embodiment of a bottom substrate.

Fig. 10 is a view of the Fig. 9 dense circuit device, spacer substrate, electrical interconnect, and bottom substrate with the interconnect clamped between the dense circuit device and the bottom substrate.

Fig. 11 is a side-section view along a depth and width dimension of the Fig. 10 dense circuit device, spacer substrate, bottom substrate, and electrical interconnect.

Fig. 12 is a view of the Fig. 5 dense circuit device, and embodiments of a spacer substrate having conductive vias, a double-sided interconnect, and a bottom substrate having circuitry.

Fig. 13 is a view of the Fig. 5 dense circuit device and spacer substrate and an embodiment of a grouped-wire interconnect and the Fig. 9 bottom substrate.

Fig. 14 is a side-section view along a depth and width dimension of the Fig. 13 dense circuit device, grouped-wire interconnect, and bottom substrate.

Fig. 15 is a view of the Fig. 13 dense circuit device, spacer substrate, and bottom substrate, and an embodiment of a grouped-wire interconnect.

Fig. 16 is a view of the Fig. 9 bottom substrate and an embodiment of a stiffened interconnect.

Fig. 17 is a view of the Fig. 16 bottom substrate and stiffened interconnect bonded to the Fig. 4 dense circuit device and spacer substrate.

The same numbers are used throughout the disclosure and figures to reference like components and features.

## DETAILED DESCRIPTION

**[0010]** The following disclosure describes various interconnects and methods for bonding them to a dense circuit device. In at least some embodiments, these interconnects and bonding methods enable electrical connection with a large, ultra-dense circuit device that allows for high conductivity and accurate pad-wire matching while also being relatively reliable, inexpensive, and production-friendly. In at least one embodiment, these interconnects and bonding methods enable low- or room-temperature bonding with a dense circuit device.

**[0011]** In at least some embodiments, the disclosed interconnects and bonding methods allow for interconnecting multiple dense circuit devices. Two dense circuit devices, for instance, can be bonded to one interconnect.

**[0012]** As used herein, the term “bonding” comprises mechanically and/or electrically connecting one structure to another. A mechanical bond, for instance, can comprise a covalent bond between a surface of one structure and a surface of another. An electrical bond is one that provides sufficient proximity to permit electrical communication. Mechanical and electrical bonds can coexist, though that is not necessary.

**[0013]** Referring initially to Figure 3, a side-section view along a depth and length dimension of a circuit device 302 is shown. The circuit device 302 comprises electrical bond pads 304 formed on outside edges of the device 302.

**[0014]** The device 302 and its bond pads 304 can comprise various types of materials. The device 302 can comprise silicon and other circuitry materials, for instance. For example, the bond pads 304 can comprise various conductors, such as gold, copper, palladium, platinum, and aluminum.

**[0015]** The device 302 and its bond pads 304 can be of various sizes, although it is to be appreciated that the Figure constitutes a diagrammatic view which is not to scale. In the ongoing example, the device 302 is square, with a length and width of about ten millimeters. The device 302 can also be from less than or about one to about twenty-five millimeters in length or width. Also in the ongoing example, the bond pads 304 are about 100 nanometers deep, 30 nanometers wide, and 100 nanometers long.

**[0016]** In one embodiment, a lower device surface 306 of the device 302 is prepared for bonding. The lower device surface 306 can be prepared for bonding using various techniques, such as mechanical abrading techniques like chemical-mechanical planarizing/polishing (CMP), and the like. The lower device surface 306 can comprise various materials, such as silicon dioxide or aluminum oxide. For this example, the device 302 comprises silicon, the bond pads 304 comprise copper, and the lower device surface 306 comprises silicon dioxide prepared and made smooth with a CMP process. The lower device

surface 306 can be made smooth enough to permit covalent bonding, which will be discussed further below.

**[0017]** The bond pads 304 can be flush with, project from, or be recessed from the lower device surface 306. In the ongoing example, the bond pads 304 are generally flush with the lower device surface 306 (as shown in Figure 3). In one embodiment, the bond pads 304 are also made smooth enough to permit covalent bonding.

**[0018]** Referring to Figure 4, in the ongoing embodiment a spacer substrate 402 is bonded to the lower device surface 306. The spacer substrate 402 has an upper surface 404 and a lower surface 406, each of which are prepared for bonding by making each smooth enough to covalently bond. The upper surface 404 and the lower surface 406 can be prepared for bonding using a CMP process, such as described above, or with other techniques such as plasma treating. The spacer substrate 402 can comprise various materials, such as aluminum dioxide or silicon. In the ongoing example, the spacer substrate 402 comprises silicon. Also in the ongoing example, the spacer substrate 402 is square and has a length and width about ten millimeters and a depth (thickness) of about 12-75 microns.

**[0019]** Referring to Figure 5, in the ongoing embodiment the spacer substrate 402 is bonded with the device 302. Once bonded, the spacer substrate 402 forms a projection from the device 302. The spacer substrate 402 and the device 302 can be bonded with heat bonding, ionic bonding, eutectic bonding, or other suitable techniques. In many cases the spacer substrate's 402 upper surface 404 and the device's 302 lower device surface 306 are not smoothed or otherwise prepared for bonding. In the ongoing example, however, the upper surface 404 of the spacer substrate 402 is smooth enough for covalent bonding and is contacted with the lower device surface 306 of the device 302 (also smooth enough for covalent bonding). At contact, the spacer substrate 402 and the device 302 covalently bond. This bonding can be performed at, for example, room temperature or at elevated temperatures. When contacted at room temperature, nearly 100 percent of possible bond strength can be

achieved over time. Over fifty percent of possible bond strength can be achieved almost instantaneously, if the applicable surfaces are smooth enough.

**[0020]** The device 302 can be fabricated such that the spacer substrate 402 is originally part of the device 302. In this implementation, the bond pads 304 are recessed from the spacer substrate's 402 projecting surface. In another implementation, the spacer substrate 402 is part of and forms a projection from a clamping or bottom substrate, discussed below.

**[0021]** The spacer substrate 402 can comprise electrically conductive vias for communication between the device 302 and a bottom substrate, also discussed below.

**[0022]** Referring to Figure 6, an interconnect 602 is oriented with respect to the device 302 such that a set of wires 604 align with the bond pads 304. Other types of interconnects can be also used, such as grouped and insulated wires, discussed below. The wires 604 can comprise various conductors such as copper, silver, gold, palladium, platinum, and aluminum. For very small wires (such as wires from one to 100 nanometers in length or diameter), highly conductive materials can aid in usability of the device 302. In the ongoing example, the wires 604 comprise copper. In one embodiment, the wires 604 are prepared smooth enough to covalently bond to the bond pads 304 using techniques discussed above.

**[0023]** In the ongoing embodiment, the interconnect 602 includes a compliant layer 606. The compliant layer 606 allows for the interconnect 602 to be compressed more easily than without it. The compliant layer 606 can include various types of compliant materials. It can also include a compliant insulator on a grouped wire, discussed in greater detail below. In the ongoing example, the compliant layer 606 comprises a polyimide.

**[0024]** In another embodiment, the device 302 is constructed to supply compliance. This can be done by choosing compliant materials in its construction or by constructing it to comprise a compliant layer (not shown).

**[0025]** The interconnect 602 can also include an intermediate layer 608 as shown. This intermediate layer 608 in the ongoing example comprises a refractory alloy, such as titanium. This intermediate layer 608 can be used as a



seed/adhesion layer for deposition of the copper in the wires 604. Thus, in some embodiments that include an intermediate layer, one characteristic that can be used to select materials of the intermediate layer can include their deposition characteristics with respect to adjacently-deposited materials.

**[0026]** The interconnect 602 and its constituent parts can be of various dimensions. In the ongoing example the wires 604 are about 200 nanometers deep, the intermediate layer 608 about 50 nanometers deep, and the compliant layer 606 about 12-75 microns deep. In the ongoing example, the total depth (thickness) of the interconnect 602 is slightly greater than that of the spacer 402. This difference allows for compression of the interconnect 602.

**[0027]** In one implementation, the interconnect 602 does not include a compliant layer. In this implementation, the spacer substrate 402 can include a compliant layer (not shown), such as between the upper surface 404 and the lower surface 406. This compliant layer can comprise a polyimide substrate.

**[0028]** In another implementation, the interconnect 602 is fabricated to surround the spacer substrate 402 to aid in orienting the wires 604 with the bond pads 304. Thus, the wires 604 of the interconnect 602 correspond to the bond pads 304 of the device 302.

**[0029]** Referring to Figure 7, a bottom plan view is shown of the bond pads 304 and the device 302 with the spacer substrate 402 attached. This bottom plan view of Figure 7 shows exemplary width and length dimensions of the pads 304. The pads 304 have a pad breadth shown generally with numeral 702. The pads 304 are separated from similarly oriented neighbors by a pad space, shown generally with numeral 704. In the ongoing example the pad breadth 702 and pad space 704 is about 30 nanometers.

**[0030]** Referring to Figure 8, a top plan view of the interconnect 602 that is designed to surround the spacer substrate 402 is shown. Here the interconnect 602 has a square hole 800 designed to fit around the spacer substrate 402. This negative of the spacer substrate's 402 projecting shape can be used to aid in orienting the interconnect 602 to the device 302. If the interconnect 602 is to be oriented with multiple dense circuit devices, the interconnect 602 can comprise multiple negatives to aid in orienting, such as with other square holes

(not shown). Other shapes of the spacer substrate 402, the device 302, and the interconnect 602 can also be used. This top plan view of Figure 8 shows width and length dimensions of the wires 604. The wires 604 have a breadth shown generally with the numeral 802. The wires 604 are separated from similarly oriented neighbors by a space, shown generally with numeral 804. The breadth 802 and the space 804, at the point where the wires 604 are to contact the pads 304, corresponds approximately with the pad breadth 702 and the pad space 704. In the ongoing example, the breadth and space 802 and 804 of the wires 604 is about 30 nanometers.

**[0031]** As shown, the wires 604 are separated with an insulator, shown generally with a numeral 806. The insulator can be air or some suitable insulative material. Use of a material as the insulator 806 can aid in future use of the interconnect 602 by providing additional structural stability for the wires 604.

**[0032]** Referring to Figure 9, in the ongoing embodiment a bottom substrate 902 is prepared for bonding with the spacer substrate 402. As mentioned previously, the lower surface 406 of the spacer substrate 402 is also prepared for bonding in this embodiment. This bottom substrate 902 can be used to clamp an interconnect, such as the interconnect 602, to a dense circuit device, such as the device 302. When used in this manner, the bottom substrate 902 acts as a clamping substrate.

**[0033]** In one embodiment, the spacer substrate 402 and/or the bottom substrate 902 comprises an adhesive. The spacer substrate 402 can comprise a depression in its upper surface 404 and/or its lower surface 406 for the adhesive. The bottom substrate 902 can comprise a depression in its upper surface 904 for the adhesive. In this embodiment, the adhesive is used to bond the spacer substrate 402 to the device 302 and/or the bottom substrate 902.

**[0034]** In another embodiment, the spacer substrate 402 and the device 302 and/or the bottom substrate 902 are configured to permit ionic bonding. In this embodiment, the spacer substrate 402 is bonded to the bottom substrate 902 and/or the device 302 using ionic bonding.

**[0035]** In the ongoing embodiment, the spacer substrate's 402 lower surface 406 and a bottom substrate upper surface 904 are made smooth enough to covalently bond. The bottom substrate upper surface 904 and the lower surface 406 can be processed using a suitable CMP process, such as described above, or with other techniques such as plasma treating. The bottom substrate upper surface 904 can comprise various materials, such as aluminum dioxide or a silicon oxide. In the ongoing example, the bottom substrate upper surface 904 comprises a silicon oxide. Also in the ongoing example, the bottom substrate 902 is about the same length and width as the device 302.

**[0036]** In another embodiment, the interconnect 602 does not include a compliant layer (not shown). In this embodiment, the spacer 402 is very slightly thinner (less deep) than the interconnect 602. This difference in thickness can be adjusted based on how compliant the device 302 and the bottom substrate 902 are to flexing away from the interconnect 602. If, for instance, the device 302 and the bottom substrate 902 are not very compliant, the thickness of the spacer 402 can be only slightly thinner than the interconnect 602. Similarly, if the device and the bottom substrate 902 are compliant, the thickness of the spacer 402 can be more than slightly thinner than the interconnect 602. The thickness of the spacer 402 can also be adjusted based on a compliance to compression of the spacer 402 and the interconnect 602. If the total compliance of these elements is fairly high, the interconnect 602 can be slightly to moderately thicker, such as even microns thicker, than a space between the device 302 and the bottom die 902 (e.g., the spacer 402). If the total compliance is low, the difference can be in a range of angstroms or nanometers.

**[0037]** It is to be appreciated and understood that each of the embodiments described above is set forth as an example, and is not intended to limit the scope or applicability of the claimed subject matter.

**[0038]** Referring to Figure 10, the interconnect 602 is bonded to the device 302 at low temperature. Low temperature comprises temperatures below 300°C. In this embodiment, the interconnect 602 is put in electrical communication (i.e., bonded) to the device 302 through physical proximity between the interconnect

602 and the device 302. In this embodiment, however, the interconnect 602 and the device 302 are not necessarily mechanically bonded to each other. Creating the electrical bond between the interconnect 602 and the device 302 can be performed and maintained with pressure. Through this pressure, the wires 604 are mechanically held, though not necessarily mechanically bonded, to the pads 304. This mechanical pressure provides sufficient proximity to enable electrical communication (e.g., an electrical bond) between the wires 604 and the pads 304. This pressure that maintains the electrical bond is created by a mechanical bond, though not necessarily between the interconnect 602 and the device 302. The mechanical bonding can be performed at low temperatures, such as room temperature. Room temperature comprises about 20°C to 50°C. This low temperature bonding can help alleviate problems associated with an interconnect and dense circuit device having different coefficients of thermal expansion. It also allows for use of high conductivity wires and wide choice in materials chosen for the wires, interconnect, and pads. In one embodiment this pressure is provided by clamping the interconnect 602 to the device 302.

**[0039]** In one implementation of this embodiment, this clamping is performed by the bottom substrate 902 being bonded to the device 302 through covalent bonding. This bonding comprises a covalent bonding of the spacer substrate 402 to either the bottom substrate 902 or the device 302, depending on whether the spacer substrate 402 was first bonded to the device 302 or the bottom substrate 902. In the ongoing example, the spacer substrate 402 is first bonded to the device 302. Then, the bottom substrate upper surface 904 is covalently bonded to the lower surface 406 of the spacer substrate 402. The bottom substrate's upper surface 904 is smooth enough for covalent bonding and is contacted with the lower surface 406, which is also smooth enough for covalent bonding. At contact the spacer substrate 402 and the bottom substrate 902 covalently bond.

**[0040]** This bonding can be performed at low temperatures to reduce problems associated with wire-pad mismatch from different CTEs in the interconnect 602 and the device 302, including room temperature. When contact is made at

room temperature, nearly 100 percent of theoretically possible bond strength can be achieved over time. Over fifty percent of theoretical possible bond strength can be achieved almost instantaneously.

**[0041]**In the ongoing embodiment the bottom substrate 902 compresses the interconnect 602. This compression is shown by an indentation in the compliant layer 606, shown generally at a numeral 1002. This compression mechanically clamps the interconnect 602 to the device 302. By so doing, the wires 604 are clamped and thus electrically bonded to the pads 304. The force for this mechanical clamping is provided by the bond of the bottom substrate 902 to the device 302, which compresses the compliant layer 606. The compliant layer 606 provides an opposite reactive force, helping to press the wires 604 to the device 302. The compliant layer 606 can be chosen with a compliance such that the compression used to put the bottom substrate 902 in contact with the device 302 is possible without breaking the device 302 or the bottom substrate 902. The compliant layer 606 can also be chosen with a material incompressible enough to provide sufficient reactive force to hold the wires 604 in electrical communication with the pads 304. The compliant layer 606 can also be constructed such that its reactive force does not dissipate so significantly over time that the electrical communication of the wires 604 to the pads 304 is lost. The compliant layer 606 also aids in the mechanical clamping of the interconnect 602 by allowing for relatively tolerant depth dimensions of the spacer 402 and/or the interconnect 602.

**[0042]**Referring to Figure 11, a side-section view along a depth and width dimension of the device 302, the interconnect 602, and the bottom substrate 902 of Figure 10 is shown. Here, the insulator 806 of Figure 8, which can be part of the interconnect 602 of Figure 10, is shown.

**[0043]**In another embodiment, a compliant layer is not used. In this embodiment, the reactive force can be provided by the wires 604 and the insulator 806 between the wires 604 (when the insulator 806 is a solid material), the device 302, the spacer substrate 402, and the bottom substrate 902, alone or in combination.

**[0044]** The interconnect systems and methods for bonding described above can, with some modification, also enable electrical connection to multiple dense circuit devices with a single interconnect.

**[0045]** Referring to Figure 12, the interconnect 602 is electrically connected to two devices, the device 302 and an embodiment of the bottom substrate 902 that comprises circuitry. In this embodiment, the interconnect 602 includes a set of bottom wires 1202 and the bottom substrate 902 comprises electrical bond pads 1204. The interconnect 602 in this embodiment also comprises another layer of the intermediate layer 608. When compressed (e.g., clamped), the bottom wires 1202 are electrically bonded to the electrical bond pads 1204. While not shown in Figure 12, the interconnect 602 can also be electrically connected to other devices, such as by being constructed to allow for additional pairs of the device 302 and the bottom substrate 902 to be connected. These additional pairs can be aligned with the interconnect 602 with aid from additional holes for placing the spacer 402, like the square hole 800 shown in Figure 8.

**[0046]** Also referring to Figure 12, the device 302 and the bottom substrate 902 can be placed into electrical communication. This can be performed using electrical vias 1206 in the spacer substrate 402. Thus, in this embodiment, after the bottom substrate 902 is bonded to the spacer 402, the device 302 and the bottom substrate 902 are placed into electrical communication.

**[0047]** The interconnect 602 is one embodiment of an electrical interconnect usable with the described interconnect system and method described above. Other types of interconnects can also be used, such as tab-flex, free wire, and ribbon cable interconnects.

**[0048]** Referring to Figure 13, a grouped-wire interconnect 1302 is bonded to the device 302. This bonding can be performed at low temperature. It can be performed by clamping the grouped-wire interconnect 1302 to the device 302, thereby creating an electrical bond through maintaining a physical force. The grouped-wire interconnect 1302 can comprise multiple insulated wires simultaneously bonded together.

**[0049]** In one embodiment the grouped-wire interconnect 1302 comprises an insulative layer 1304. The interconnect 1302 is clamped by the bottom substrate 902 by being bonded to the device 302 through low-temperature covalent bonding. This covalent bonding can comprise a covalent bonding of the spacer substrate 402 to either the bottom substrate 902 or the device 302, depending on whether the spacer substrate 402 is first bonded to the device 302 or the bottom substrate 902. This covalent bonding can be performed at room temperature to reduce problems associated with wire-pad mismatch from different CTEs in the grouped-wire interconnect 1302 and the device 302. Thus, this covalent bonding of the interconnect 1302 to the device 302 enables an electrical bond between the wires 604 and the bond pads 304.

**[0050]** In the ongoing embodiment the device 302 and the bottom substrate 902 compress the grouped-wire interconnect 1302 once the bottom substrate 902 is bonded to the device 302. A material allowing compliance can be included between edges of the device 302 and the bottom substrate 902. In one implementation, an embodiment of the compliant layer 606 is used, shown in Figure 13.

**[0051]** Referring to Figure 14, a depth and length side-sectional view of the device 302, the grouped-wire interconnect 1302, and the bottom substrate 902, all of Figure 13, is shown. Here, the compliant layer 606 is also shown. A guide can also be used to confine the wires 604 with the bond pads 304, shown at numeral 1402, while the interconnect 1302 is being clamped.

**[0052]** In this example, the insulative layer 1304 can be used to set a grouped-wire space 1404 between the wires 604. This space 1404 can be about twice the thickness of the insulative layer 1304.

**[0053]** Referring to Figure 15, a depth and width side-section of the device 302, the grouped-wire interconnect 1302, and the insulative layer 1304 is shown. In this embodiment, the insulative layer 1304 of the wires 604 of the grouped-wire interconnect 1302 acts as a compliant material.

**[0054]** In another embodiment, a compliant layer is not used. In this embodiment, the compliance and reactive force is provided by the wires 604 of

the grouped-wire interconnect 1302, the device 302, the spacer substrate 402, and the bottom substrate 902, alone or in combination.

**[0055]** The interconnect 602 and the grouped-wire interconnect 1302 are two embodiments of an electrical interconnect usable with the described interconnect system and method described above, though other embodiments and modifications of these interconnects can also be used.

**[0056]** Referring to Figure 16, a depth and length side-section view of an embodiment of a stiffened interconnect 1602 and the bottom substrate 902 is shown. The stiffened interconnect 1602 comprises an embodiment of the wires 604, the compliant layer 606, the intermediate layer 608, and a stiffening layer 1604. Especially when an interconnect has thin layers, such as a total thickness (shown along the depth dimension of Figure 16) of less than one thousand nanometers, the interconnect may be flexible. In this embodiment of Figure 16, the stiffening layer 1604 acts to stiffen the interconnect 1602. The stiffness provided by the stiffening layer 1604 can aid in orienting the wires 604 with the electrical bond pads 304 (such as those shown in Figure 3). The stiffening layer 1604 can be of various thicknesses and materials. In the example given in Figure 16, the stiffening layer 1604 comprises silicon of a few microns thickness.

**[0057]** In this example, a bonding surface 1606 of the stiffening layer 1604 can be prepared for bonding. The interconnect 1602 and the bottom substrate 902 can be bonded in various ways known in the art or can be created as one unit. In the ongoing example the bonding surface 1606 is made smooth enough to covalently bond with the surface 904 of the bottom substrate 902. In the ongoing example the bottom substrate 902 is bonded covalently to the surface 904.

**[0058]** A depression surface 1608 in a depression in the stiffened interconnect 1602 is prepared for bonding. This preparation can include smoothing for covalent bonding.

**[0059]** Referring to Figure 17, a side-section view of the circuit device 302, the spacer substrate 402, the stiffened interconnect 1602, and the bottom substrate 902 is shown. The bottom substrate 902 and the device 302 can be bonded at



low temperature, such as room temperature. In one embodiment, the bottom substrate 902 and the device 302 are bonded at room temperature by covalently bonding the depression surface 1608 of the stiffening layer 1604 (which is at a depression in the stiffened interconnect 1602) with a bottom surface 406 of the spacer substrate 402 that has already been bonded or is part of the device 302.

**[0060]** In at least one embodiment, the device 302 is bonded (via clamping) to the stiffened interconnect 1602 after the spacer substrate 402 is bonded to the stiffening layer 1604. In this embodiment, the spacer substrate 402 is then bonded covalently via the upper surface 404 of the spacer substrate 402 and the lower device surface 306 of the device 302. By so doing, the device 302 is electrically bonded to the stiffened interconnect 1602. Following this, the bottom substrate 902 can be bonded to the stiffened interconnect 1602 to provide additional structural strength or compression.

**[0061]** In each of these embodiments, the interconnect 1602 is pressed to the device 302. This pressure provides the mechanical compression to provide electrical communication between the wires 604 to the bond pads 304. The reactive force and compliance in these embodiments is provided in part by the compliant layer 606, also shown in Figure 17.

**[0062]** Following the bonding of the various interconnects to the devices above, the devices and the interconnect can be cyclically heated to reduce possible strain between the devices and/or the interconnect. This cyclical heating can also aid in or create bonding between wires of the interconnect and pads of the device(s).

**[063]** Although the invention is described in language specific to structural features and methodological steps, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or steps described. Rather, the specific features and steps disclosed represent exemplary forms of implementing the claimed invention.

What is Claimed is: